REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R057-92.	91-11-18	Michael A. Frye
B	Drawing updated to reflect current requirements. - lgt	01-12-07	Raymond Monnin

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

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REV STATUS				REV			B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Rick C. Officer	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43216** **http://www.dscc.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Charles E. Besore	
	APPROVED BY Michael A. Frye	MICROCIRCUIT, LINEAR, 16-BIT, VOLTAGE OUTPUT DAC, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 03 April 1990	
	REVISION LEVEL B	SIZE A CAGE CODE **67268** **5962-89697**
		SHEET 1 OF 14

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-89697	01	X	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD7846	L^2CMOS 16-bit voltage output DAC

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Positive supply voltage to DGND (V_{DD}) ..... -0.3 V dc to +17 V dc
Positive logic supply voltage to DGND (V_{CC}) ..... -0.3 V dc to +7.0 V dc
Negative supply voltage to DGND (V_{SS}) ..... +0.3 V dc to -17 V dc
V_{REF+} to DGND ..... ±25 V dc
V_{REF-} to DGND ..... ±25 V dc
V_{OUT} to DGND ..... ±25 V dc 1/
R_{IN} to DGND ..... ±25 V dc
Logic input voltage to DGND ..... -0.3 V dc to V_{CC} +0.3 V dc
Logic output voltage to DGND ..... -0.3 V dc to V_{CC} +0.3 V dc
Storage temperature range ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Power dissipation to 75°C (P_D) ..... 1000 mW 2/
Thermal resistance, junction to case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +150°C

1.4 Recommended operating conditions.

Negative supply voltage (V_{SS}) ..... -14.25 V dc to –15.75 V dc
Positive supply voltage (V_{DD}) ..... +14.25 V dc to +15.75 V dc
Positive logic supply voltage (V_{CC}) ..... +4.75 V dc to +5.25 V dc
Ambient operating temperature range (T_A) ..... -55°C to +125°C

1/ V_{OUT} may be shorted to DGND, V_{DD}, V_{SS}, V_{CC} provided that the power dissipation of the package is not exceeded.
2/ Derates above T_A = +75°C at 10 mW/°C.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 -- Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 -- List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Output voltage ranges. The output voltage ranges shall be as specified on figure 3.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 4.

3.2.5 Switching characteristics. The switching characteristics shall be as specified on figure 5.

3.2.6 Load circuits. The load circuits shall be as specified on figure 6.

3.2.7 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution	RES		1, 2, 3	01	16		Bits
Relative accuracy	R_A	Unipolar output 2/	1, 2, 3	01	-16	+16	LSB
Differential nonlinearity 3/	DNL		1, 2, 3	01	-1	+1	
Gain error 4/	A_E		1	01	-16	+16	
			2, 3		-24	+24	
Offset error	O_E		1	01	-16	+16	
			2, 3		-24	+24	
Relative accuracy	R_A	Bipolar output 5/	1, 2, 3	01	-8	+8	LSB
Differential nonlinearity 3/	DNL		1, 2, 3	01	-1	+1	
Gain error 4/	A_E		1	01	-8	+8	
			2, 3		-16	+16	
Offset error 4/	O_E		1	01	-8	+8	
			2, 3		-16	+16	
Bipolar zero error	BIP_e		1	01	-8	+8	
			2, 3		-16	+16	
Reference input resistance	R_{REFIN}	Resistance from V_{REF-} to V_{REF+}	1, 2, 3	01	20	40	kΩ
V_{REF+} range 6/	V_{REF+}		1, 2, 3	01	V_{SS} +6.0	V_{DD} -6.0	V
V_{REF-} range 6/	V_{REF-}		1, 2, 3	01	V_{SS} +6.0	V_{DD} -6.0	V
Output swing voltage 6/	V_{SWING}		1, 2, 3	01	V_{SS} +4.0	V_{DD} -3.0	V
Input voltage high level	V_{IH}		7, 8	01	2.4		V
Input voltage low level	V_{IL}		7, 8	01		0.8	V
Digital input current	I_{IN}		1, 2, 3	01		±10	μA
Output voltage high level	V_{OH}	I_{SOURCE} = 400 μA	1, 2, 3	01	4.0		V
Output voltage low level	V_{OL}	I_{SINK} = 1.6 mA	1, 2, 3	01		0.4	V
Floating state leakage current	I_{LKG}	$DB_0 - DB_{15}$ = 0 to V_{CC} V	1, 2, 3	01		±10	μA
Positive power supply current	I_{DD}	V_{OUT} unloaded 7/	1, 2, 3	01		5.0	mA
Negative power supply current	I_{SS}					5.0	
Positive logic supply current	I_{CC}					1.0	
Power supply sensitivity 8/	PSS					2.0	LSB/V
Floating state output capacitance	C_{OUT}	See 4.3.1 c	4	01		10	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Digital input capacitance	C_{IN}	See 4.3.1 c	4	01		10	pF
Functional test		See 4.3.1 d	7, 8	01			
R/$\overline{W}$ to $\overline{CS}$ setup time	t_1	See figure 5 9/	9	01	40		ns
			10, 11		50		
$\overline{CS}$ pulse width (write cycle)	t_2		9	01	150		
			10, 11		190		
R/$\overline{W}$ to $\overline{CS}$ hold time	t_3		9	01	40		
			10, 11		50		
Data setup time	t_4		9	01	110		
			10, 11		120		
Data hold time	t_5		9, 10, 11	01	0		
Data access time 10/	t_6		9	01		230	
			10, 11			320	
Bus relinquish 11/	t_7		9	01	10	80	
			10, 11		10	90	
$\overline{CLR}$ setup time	t_8		9, 10, 11	01	20		
$\overline{CLR}$ pulse width	t_9		9, 10, 11	01	150		
$\overline{CLR}$ hold time	t_{10}		9, 10, 11	01	0		
$\overline{LDAC}$ pulse width	t_{11}		9	01	80		
			10, 11		100		
$\overline{CS}$ pulse width (read cycle)	t_{12}		9	01	240		
			10, 11		330		

1/ Unless otherwise specified, 14.25 V dc $\le V_{DD} \le$ 15.75 V dc, -14.25 V dc $\le V_{SS} \le$ -15.75 V dc and 4.75 V dc $\le V_{CC} \le$ 5.25 V dc. V_{OUT} loaded with 3 kΩ, 1000 pF to 0 V. V_{REF+} = +5.0 V dc, R_{IN} = connected to 0 V.
2/ V_{REF-} = 0 V, V_{OUT} = 0 V to 10 V, 1 LSB = 153 μV.
3/ Monotonicity is guaranteed over full temperature range.
4/ V_{OUT} load = 10 MΩ.
5/ V_{REF} = -5.0 V, V_{OUT} = -10 V to +10 V, 1 LSB = 305 μV.
6/ If not tested, shall be guaranteed to the limits specified in table I herein.
7/ The device is functional with a power supply of ±12 V.
8/ Sensitivity of gain error, offset error and bipolar zero error to V_{DD}, V_{SS} variations.
9/ All input control signals are specified with $t_R = t_F$ = 5.0 ns (10 % to 90 % of +5.0 V) and timed from a voltage level of 1.6 V.
10/ t_6 is measured with the load circuits for access time on figure 6 and defined as the time required for an output to cross 0.8 V or 2.4 V.
11/ t_7 is defined as the time required for an output to change 0.5 V when loaded with the circuits for bus relinquish time on figure 6.

Device type	01
Case outline	X and 3
Terminal number	Terminal symbol
1	DB_2
2	DB_1
3	DB_0
4	V_{DD}
5	V_{OUT}
6	R_{IN}
7	V_{REF+}
8	V_{REF-}
9	V_{SS}
10	DB_{15}
11	DB_{14}
12	DB_{13}
13	DB_{12}
14	DB_{11}
15	DB_{10}
16	DB_9
17	DB_8
18	DB_7
19	DB_6
20	DGND
21	V_{CC}
22	R/$\overline{W}$
23	$\overline{CS}$
24	$\overline{CLR}$
25	$\overline{LDAC}$
26	DB_5
27	DB_4
28	DB_3

FIGURE 1. Terminal connections.

$\overline{CS}$	R/$\overline{W}$	$\overline{LDAC}$	$\overline{CLR}$	Function
1	X	X	X	3-state DAC I/O latch in high-Z state
0	0	X	X	DAC I/O latch loaded with DB_{15}–DB_0
0	1	X	X	Contents of DAC I/O latch available on DB_{15}–DB_0
X	X	0	1	Contents of DAC I/O latch transferred to DAC latch
X	0	X	0	DAC latch loaded with 000 … 000
X	1	X	0	DAC latch loaded with 100 … 000

0 = Low
1 = High
X = Don’t care

FIGURE 2. Truth table.

Output range	V_{REF+}	V_{REF-}	R_{IN}
0 V to +5.0 V	+5.0 V	0 V	V_{OUT}
0 V to +10 V	+5.0 V	0 V	0 V
+5.0 V to –5.0 V	+5.0 V	–5.0 V	V_{OUT}
+5.0 V to –5.0 V	+5.0 V	0 V	+5.0 V
+10 V to –10 V	+5.0 V	–5.0 V	0 V

FIGURE 3. Output voltage ranges.

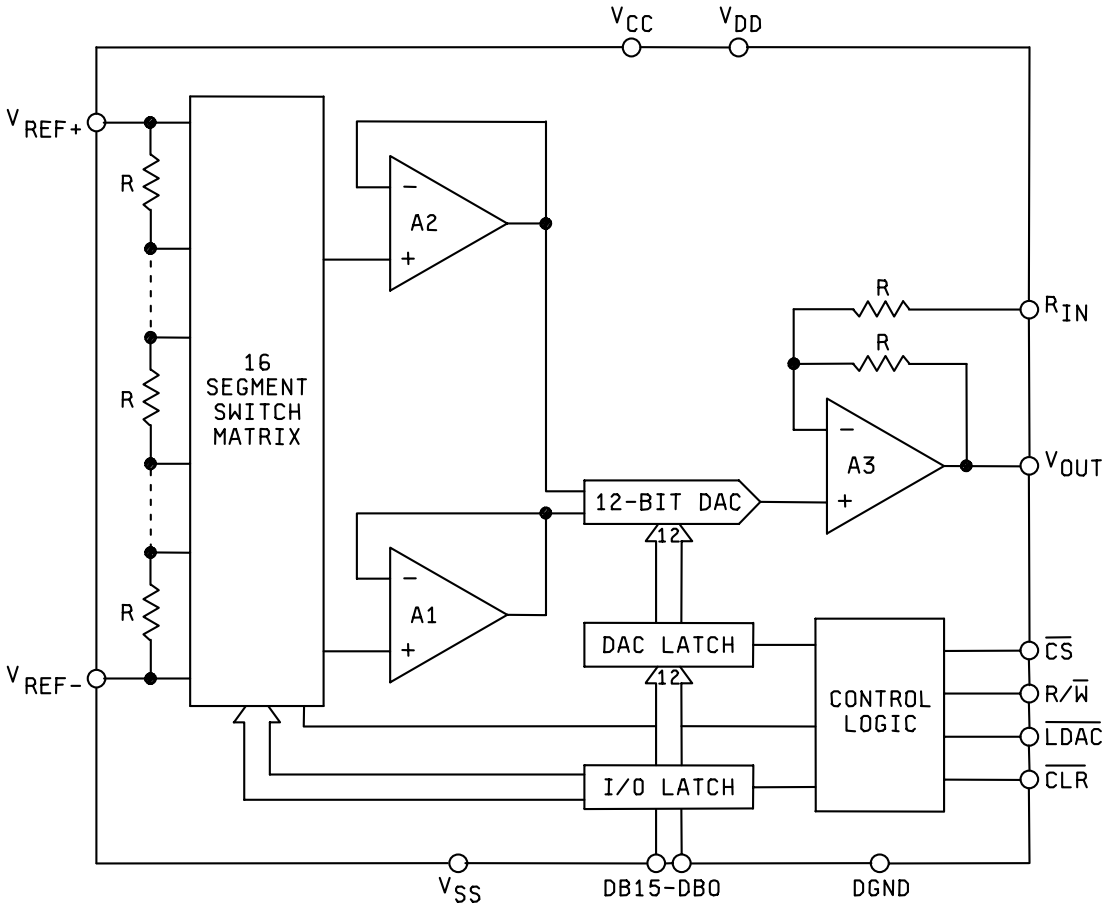


FIGURE 4. Logic diagram.

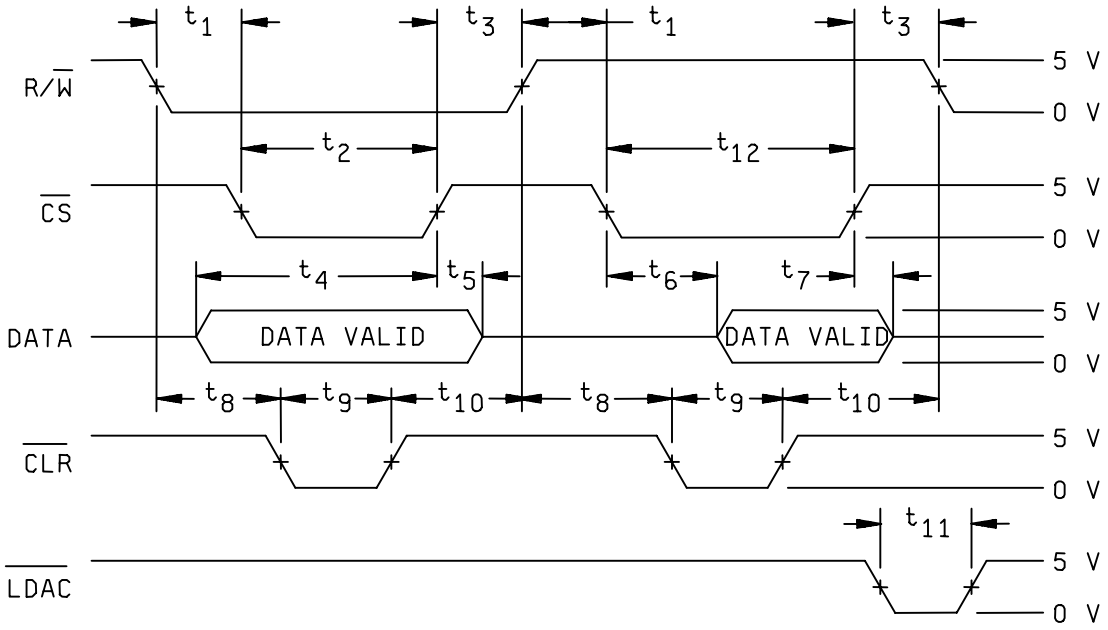
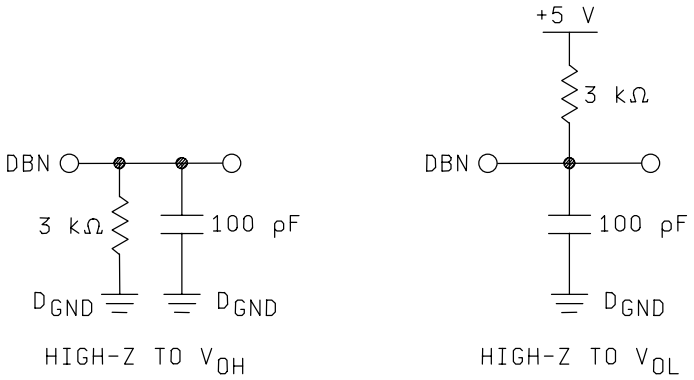


FIGURE 5. Switching characteristics.

LOAD CIRCUITS FOR ACCESS TIME (T_6)



LOAD CIRCUITS FOR BUS RELINQUISH TIME (T_7)

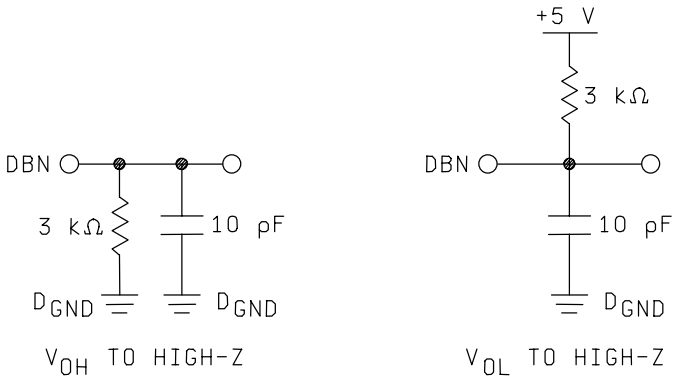


FIGURE 6. Load circuits.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits specified in table I herein.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Pin description. The pin description is as follows.

Pin	Description
DB_2 - DB_0	Data I/O pins. DB_0 is LSB.
V_{DD}	Positive supply for analog circuitry. This is a +15 V nominal.
V_{OUT}	DAC output voltage pin.
R_{IN}	Input to summing resistor of DAC output amplifier. This is used to select output voltage ranges. See figure 2.
V_{REF+}	V_{REF+} input. The DAC is specified for V_{REF+} = +5.0 V.
V_{REF-}	V_{REF-} input. For unipolar operation connect V_{REF-} to 0 V and for bipolar operation connect it to –5.0 V. The device is specified for both conditions.
V_{SS}	Negative supply for analog circuitry. This is –15 V nominal.
DB_{15} – DB_6	Data I/O pins. DB_{15} is MSB.
DGND	Ground pin for logic circuitry.
V_{CC}	Positive supply for logic circuitry. This is +5 V nominal.
R/$\overline{W}$	R/$\overline{W}$ input. This can be used to load data to the DAC or to read back the DAC latch contents.
$\overline{CS}$	Chip select input. This selects the device.
$\overline{CLR}$	Clear input. The DAC can be cleared to 000…000 or 100…000. See figure 2.
$\overline{LDAC}$	Asynchronous load input to DAC.
DB_5 – DB_3	Data I/O pins.

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-12-07

Approved sources of supply for SMD 5962-89697 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8969701XA	24355	AD7846SQ/883B
5962-89697013A	24355	AD7846SE/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices, Inc. Rt. 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of Contact: Bay F-1 Raheen Ind. Estate Limerick, Ireland

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.